	Search Text
1	density same (check$4 evaluat$5 verif$6) same (ic chip circuit)
2	density same (check$4 evaluat$5 verif$7) same (ic chip circuit) and @ad<"20040326"
3	density same (check$4 evaluat$5 verif$7) same (ic chip circuit) and @ad<"20040326" and (window box tile) with (siz$4 interval gnaularity resolution)
4	density same (check$4 evaluat$5 verif$7) same (ic chip circuit) and @ad<"20040326" and (window box) with (siz$4 tile resolution) and (shape geometry) same (populat$5 distibut$4 uniform$5)
5	density same (check$4 evaluat$5 verif$7) same (ic chip circuit) and @ad<"20040326" and (window box tile) with (siz$4 dimension resolution) and (shape geometry) same (populat$5 distibut$4 uniform$5)
6	density same (check$4 evaluat$5 verif$7) same (ic chip circuit) and @ad<"20040326" and (window box tile) with (evaluat$5 granular$6)
7	density same (check$4 evaluat$5 verif$7) same (ic chip circuit) and @ad<"20040326" and (window box tile) with (evaluat$5 granular$6) and (window box tile) with (granular$6)
8	density same (check$4 evaluat$5 verif$7) same (ic chip circuit) and @ad<"20040326" and (window box tile) with (evaluat$5 granular$6) and (square) with (granular$6)
9	density same (check$4 evaluat$5 verif$7) same (ic chip circuit) and @ad<"20040326" and (window box tile) with (evaluat$5 granular$6) and (window box tile) with (siz$4 dimension resolution$4)
10	density same (check$4 evaluat$5 verif$7) same (ic chip circuit) and @ad<"20040326" and (window box tile) with (evaluat$5 granular$6) and (window box tile) with (siz$4 dimension resolution$4) and (smallest lowest) with (sub array resolution granular$5)
11	(populat$5) same (check$4 evaluat$5 verif$7) same (ic chip circuit) and @ad<"20040326" and (window box tile) with (evaluat$5 granular$6) and (window box tile) with (siz$4 dimension resolution$4) and (smallest lowest) with (sub array resolution granular$5)
12	(populat$5 density) same (check$4 evaluat$5 verif$7) same (ic chip circuit) and @ad<"20040326" and (window box tile) with (evaluat$5 granular$6) and (window box tile) with (siz$4 dimension resolution$4) and (smallest lowest) with (sub window array resolution granular$5)
13	"20040044979"
14	(populat$5 density) same (check$4 evaluat$5 verif$7 distribut$4) same (ic chip circuit die) and @ad<"20040326" and trapezoid$4
15	(populat$5 density) same (check$4 evaluat$5 verif$7 distribut$4) same (ic chip circuit die) same trapezoid$4 and @ad<"20040326"
16	(populat$5 density) same (check$4 evaluat$5 verif$7 distribut$4) same (ic chip circuit die substrate) and grid$4 and @ad<"20040326"
17	(populat$5 density) same (check$4 evaluat$5 verif$7 distribut$4) same (ic chip circuit die substrate) and grid$4 and @ad<"20040326" and (divi$6 granular$6 window box tile) with (siz$4 dimension resolution$4 grid$4)
18	(populat$5 density) same (check$4 evaluat$5 verif$7 distribut$4) same (ic chip circuit die substrate) and grid$4 and @ad<"20040326" and (divi$6 granular$6 window box tile) with (siz$4 dimension resolution$4 grid$4) and "716"/$.ccls.

	Search Text
19	(populat$5 density) same (check$4 evaluat$5 verif$7 distribut$4) same (ic chip circuit die substrate) and grid$4 and @ad<"20040326" and (divi$6 granular$6 window box tile) with (siz$4 dimension resolution$4 grid$4) and (shape geometry dimension$4 siz$4) same (populat$5 density) same (check$4 evaluat$5 verif$7 distribut$4)
20	(populat$5 density) same (check$4 evaluat$5 verif$7 distribut$4) same (ic chip circuit die substrate) and grid$4 and @ad<"20040326" and (divi$6 granular$6 window box tile) with (siz$4 dimension resolution$4 grid$4) and (shape geometry dimension$4 siz$4) same (populat$5 density) same (check$4 evaluat$5 verif$7 distribut$4) and "716"/$.ccls.
21	(populat$5 density) same (check$4 evaluat$5 verif$7 distribut$4) same (ic chip circuit die substrate) and grid$4 and @ad<"20040326" and (divi$6 granular$6 window box tile) with (siz$4 dimension resolution$4 grid$4) and (shape geometry dimension$4 siz$4) same (populat$5 density) same (check$4 evaluat$5 verif$7 distribut$4) and (array subarray rule)
22	(populat$5 density) same (check$4 evaluat$5 verif$7 distribut$4) same (ic chip circuit die substrate) and grid$4 and @ad<"20040326" and (divi$6 granular$6 window box tile) with (siz$4 dimension resolution$4 grid$4) and (shape geometry dimension$4 siz$4) same (populat$5 density) same (check$4 evaluat$5 verif$7 distribut$4) and (array subarray rule) and "716"/$.ccls.
23	(DRC design with rule with check$4) and (populat$5 density) same (check$4 evaluat$5 verif$7 distribut$4) same (ic chip circuit die substrate) and grid$4 and @ad<"20040326" and (divi$6 granular$6 window box tile) with (siz$4 dimension resolution$4 grid$4) and (shape geometry dimension$4 siz$4) same (populat$5 density) same (check$4 evaluat$5 verif$7 distribut$4)
24	(lithograph$6 photolithograph$6 microlithograph$6) and (populat$5 density) same (test$4 check$4 evaluat$5 verif$7 distribut$4) same (ic chip circuit die substrate wafer) and (DRC design with rule with check$4) and grid$4 and @ad<"20040326" and (divi$6 granular$6 window box tile) with (siz$4 dimension resolution$4 grid$4) and (shape geometry dimension$4 siz$4) same (populat$5 density) same (check$4 evaluat$5 verif$7 distribut$4)
25	(lithograph$6 photolithograph$6 microlithograph$6 DRC design with rule with check$4) and (populat$5 density) same (test$4 check$4 evaluat$5 verif$7 distribut$4) same (ic chip circuit die substrate wafer) and (grid$4 window) and @ad<"20040326" and (divi$6 granular$6 window box tile) with (siz$4 dimension resolution$4 grid$4) and (shape geometry dimension$4 siz$4) same (populat$5 density) same (check$4 evaluat$5 verif$7 distribut$4)